Xserve G5 Developer Note

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Introduction to Xserve G5 Developer Note

This developer note describes Apple Computer's Xserve G5. The note provides information about the internal design of the computer, its input-output and expansion capabilities, and issues affecting compatibility.

This developer note is intended to help hardware and software developers design products that are compatible with the Macintosh products described here. If you are not already familiar with Macintosh computers or if you would simply like additional technical information, refer to Chapter A, "Supplemental Reference Documents." (page 45)

Organization of This Document

The information is arranged in four chapters and two appendixes:

- Chapter 1, "Overview of the Xserve G5", (page 11) gives a summary of the features of the Xserve G5, describes the physical appearance of the enclosure, and lists compatibility issues of interest to developers.

- Chapter 2, "Architecture", (page 21) describes the internal organization of the computer. It includes a functional block diagram and descriptions of the main components on the logic board.

- Chapter 3, "Input and Output Devices", (page 31) describes the built-in I/O devices and the external I/O ports.

- Chapter 4, "Expansion", (page 41) describes the expansion slots on the logic board and provides specifications for the expansion modules.

- Appendix A, "Supplemental Reference Documents", (page 45) provides sources of additional information about the technologies used in the Xserve G5 computer.

- Appendix B, "Conventions and Abbreviations", (page 51) lists standard units of measure and other abbreviations used in this developer note.

Overview of the Xserve G5

The Xserve G5 is the Macintosh server platform using the PowerPC G5 microprocessor. It has a rack-mount enclosure and includes server-oriented features such as ample internal storage, hot-pluggable drives, hardware monitoring, and easy tool access.

This developer note includes both the standard three drive bay configuration and the basic cluster node single drive bay configuration. Both configurations feature high performance I/O, high speed network I/O, and 400 MHz ECC DDR memory. The differences in the two Xserve G5 configurations are identified throughout this document. When not specifically stated, the information presented in this note is for the both configurations.

Hardware Features

Table 1-1 (page 11) below, provides a list of the hardware features of the Xserve G5 and Table 1-2 (page 12) provides a list of the hardware features of the Xserve G5 cluster node configuration. New features are listed first. Each of the major features is described more fully later in this note, as indicated by the cross references.

Table 1-1   Hardware Features of the Xserve G5

	New Features
Microprocessor speed	Single 2.0 GHz or dual 2.3 GHz PowerPC G5 microprocessors. See "PowerPC G5 Microprocessor" (page 23).
Optical drive	Contains a Combo (CD-RW/DVD-ROM) drive; see "Combo Drive" (page 37). A SuperDrive (CD-RW/DVD-RW) is available as a build-to-order option; see "SuperDrive (Optional)" (page 38).
RAM	Eight slots (four pairs of two) for 184-pin DIMMs (dual inline memory modules) using ECC (error correcting code) DDR400 (double data rate) dynamic RAM devices. Supports a maximum of 8 GB. See "RAM Expansion" (page 41).
Hard disk	7200-rpm, hot-pluggable, 80 GB hard disk drive with 8MB cache in one of the three drive bays. Build-to-order 250 GB or 400 GB drives available for a maximum of 1.2 TB internal storage.

	Additional Features
Hyper Transport	A high-speed bus architecture between the memory controller and device I/O. For more information, see "HyperTransport Technology" (page 25).
Processor system bus	64-bit processor interface bus running at half the speed of the system microprocessor. See "Processor Bus" (page 24).
Memory caches	Internal 512 KB level 2 cache per processor. See "Cache Memory" (page 23).
ROM	ROM-in-RAM implementation with 2 MB of boot ROM. For information about the ROM, see "Boot ROM" (page 27). For information about the ROM-in-RAM implementation, see the references listed in "ROM-in-RAM Architecture" (page 46).
Hard disk drive bays	Up to three drive bays for serial ATA (SATA) drives with independent buses and support for hot-pluggable drives using Apple Drive Modules. See "Hard Disk Drives" (page 38).
USB 2.0 ports	Two USB 2.0 ports. See "USB Ports" (page 31).
Ethernet	Dual Ethernet ports for 10Base-T, 100Base-T, or 1000Base-T operation. See "Ethernet Ports" (page 35).
FireWire ports	Two FireWire 800 ports on back panel and one FireWire 400 on front. See "FireWire Ports" (page 32).
PCI-X card expansion slots	Two PCI-X expansion slots for PCI or PCI-X cards. See "PCI or PCI-X Expansion Slots" (page 25).
System Monitoring	The system monitors the fan speeds and reports if speeds are outside acceptable range, indicating that a fan needs service.

Table 1-2   Hardware Features of the Cluster Node Xserve G5

	New Features
Microprocessor speed	Dual 2.3 GHz PowerPC G5 microprocessors. See "PowerPC G5 Microprocessor" (page 23).
RAM	Eight slots (four pairs of two) for 184-pin DIMMs (dual inline memory modules) using ECC (error correcting code) DDR400 (double data rate) dynamic RAM devices. Supports a maximum of 8 GB. See "RAM Expansion" (page 41).
	Additional Features
Memory caches	Internal 512 KB level 2 cache per processor. See "Cache Memory" (page 23).
Processor system bus	64-bit processor interface bus running at half the speed of the system microprocessor. See "Processor Bus" (page 24).

Hyper Transport	A high-speed bus architecture between the memory controller and device I/O. For more information, see "HyperTransport Technology" (page 25)
ROM	ROM-in-RAM implementation with 2 MB of boot ROM. For information about the ROM, see "Boot ROM" (page 27). For information about the ROM-in-RAM implementation, see the references listed in "ROM-in-RAM Architecture" (page 46).
Hard disk drive bay	One serial ATA (SATA) Apple Drive Module with support for hot-pluggable drive. See "Hard Disk Drives" (page 38).
Hard disk	7200-rpm, hot-pluggable, 80 GB hard disk drive with 8MB cache. Build-to-order 250 GB or 400 GB drives available.
USB 2.0 ports	Two USB 2.0 ports. See "USB Ports" (page 31).
Ethernet	Two Ethernet ports for 10Base-T, 100Base-T, or 1000Base-T operation. See "Ethernet Ports" (page 35).
FireWire ports	Two FireWire 800 ports on back panel and one FireWire 400 on front. See "FireWire Ports" (page 32).
PCI-X card expansion slots	Two PCI-X expansion slots for PCI or PCI-X cards. See "PCI or PCI-X Expansion Slots" (page 25).
System Monitoring	The system monitors the fan speeds and reports if speeds are outside acceptable range, indicating that a fan needs service.

Features of the Enclosure

The Xserve G5 has a rack optimized enclosure that is 1U (1.75" tall) and conforms to the industry standard for 19-inch rack mounting. For information about the standard, see the reference at "EIA Rack Standards" (page 48).

All of the components in the server are accessible without the use of special tools.

Figure 1-1 (page 14) shows the front panel of the standard Xserve G5, which has a power button and light, an enclosure lock and status light, a system identifier button and light, a FireWire 400 port, Ethernet link lights, a slot-loading optical drive, up to three serial ATA drive modules, and a two-by-eight set of system activity lights.

> **Note:** Depending on the configuration of your Xserve G5, the appearance may differ slightly from the illustrations.

Figure 1-1   Xserve G5 slot load front panel
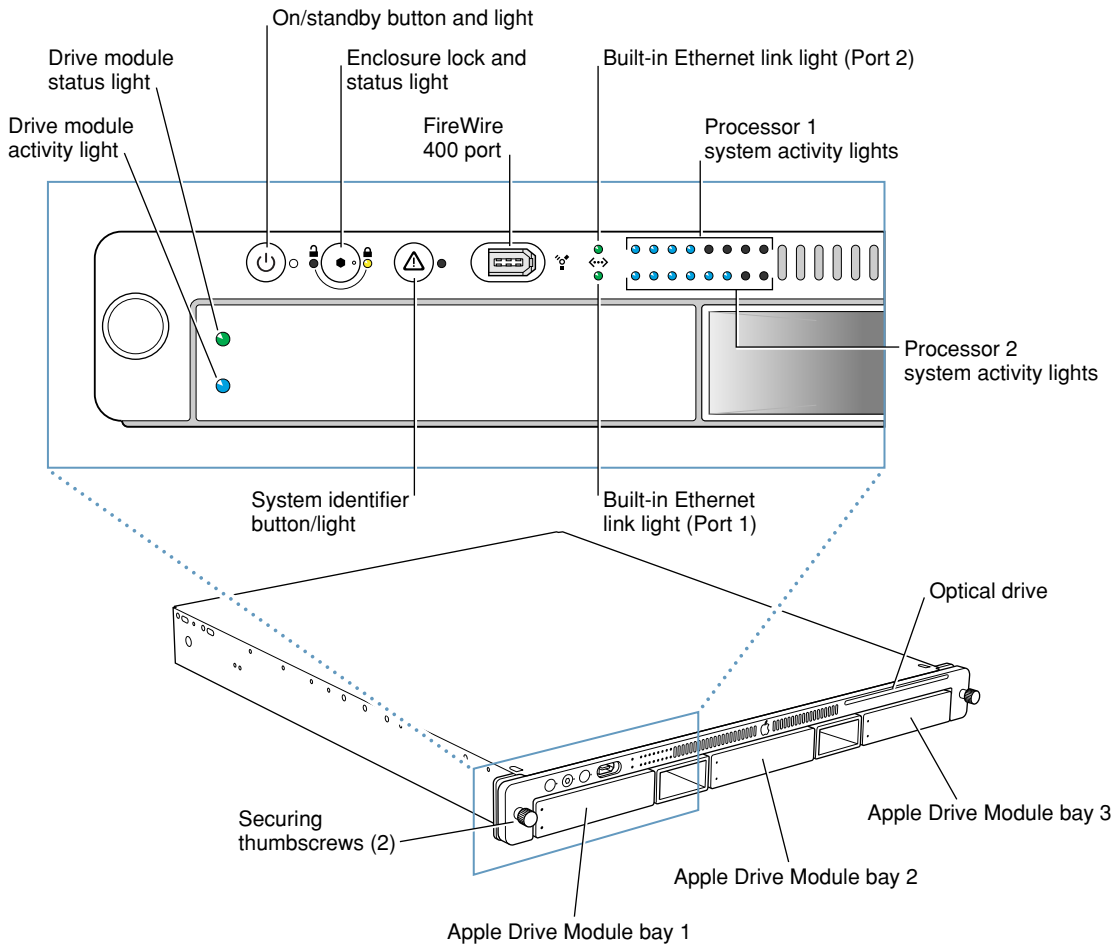
Figure 1-2 (page 15) shows the back panel of the slot load and cluster node Xserve G5, which are basically the same. The back panel has an A/C power socket, two gigabit Ethernet ports, two FireWire 800 ports, a system identifier button and light, two USB 2.0 ports, a serial console port, and two PCI-X card slots. An optional video card can occupy one of the PCI-X slots in the standard configuration (not supported in the cluster node configuration).

Figure 1-2   Xserve G5 slot load and cluster node back panel

Gigabit Ethernet port(s)

Power socket   Ethernet activity lights   PCI-X card expansion slots (2)

USB ports (2)

Ethernet link lights   FireWire 800 ports (2)

System identifier button/light   Serial console port
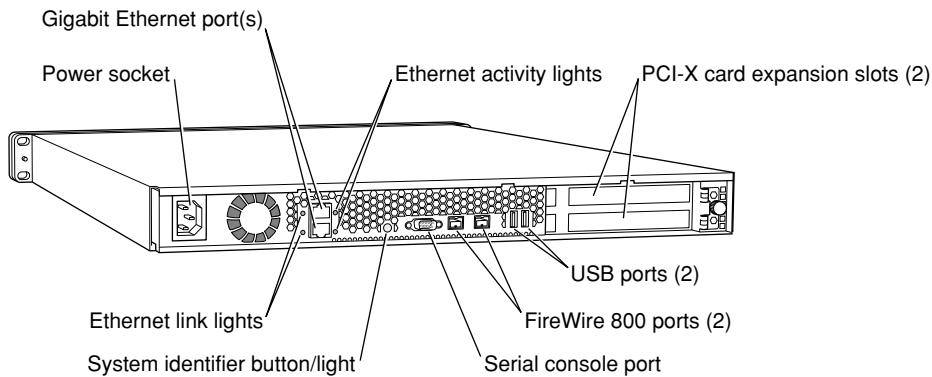
Figure 1-3 (page 15) shows the front panel of the cluster node Xserve G5, which has a power button and light, an enclosure lock and status light, a system identifier button and light, a FireWire 400 port, two Ethernet link lights, a two-by-eight set of system activity lights, and drive module and lights. Additional drive modules cannot be installed in the cluster node configuration. The rear panel is mostly the same as the slot load configuration and is shown in Figure 1-2 (page 15).

Figure 1-3   Xserve G5 cluster node front panel

System identifier button/light

Enclosure lock and status light   FireWire 400 port

On/standby button and light   Built-in Ethernet link light (Port 2)

Processor 1
system activity lights

Securing thumbscrews (2)   Processor 2
system activity lights

Built-in Ethernet link light (Port 1)

Apple Drive Module bay

Drive module status light

Drive module activity light
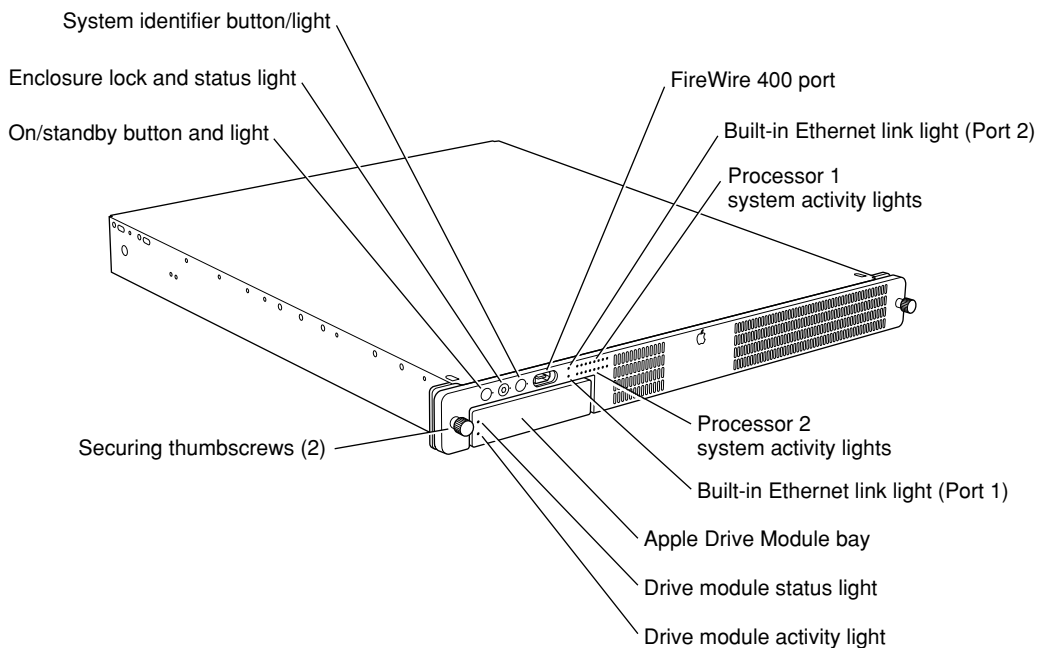
System Activity Lights Definitions

The system identifier button on the server's front panel can be used to initiate a limited number of firmware boot commands without connecting a keyboard or monitor. For instructions on entering the commands, refer to the *Xserve G5 User's Guide* that shipped with your computer.

The bottom row of system activity lights on the Xserve G5 (shown in Figure 1-1 (page 14) and Figure 1-3 (page 15) indicates the state of the computer when commands are entered and during normal operation. The lights are referenced from right to left, with light one being the rightmost and light 8 being the leftmost. The bottom row of system activity lights are defined below in Table 1-3.

Table 1-3   Definition of System Activity Lights

Light 1(far right)	Start up from a system disc in the optical drive (also ejects a disc already in the optical drive).
Light 2	Start up from a network server (NetBoot).
Light 3	Start up from the internal drive (leftmost drive if more than one).
Light 4	Bypass the current startup disk and start up from any other available startup disk.
Light 5	Begin target disk mode (all drives, including the optical drive, will show up).
Light 6	Restore the system's default settings (reset NVRAM).
Light 7	Enter Open Firmware (via the serial port if no monitor and keyboard are connected).
Light 8	Put the system into diagnostic hardware test mode.

Note: If Open Firmware Security is turned on, front panel mode is not available. In this case, the two rows of system activity lights flash twice when you try to enter a command with the system identifier and the system resumes its regular startup sequence.

System Software

The Xserve G5 comes with Mac OS X Server installed. The Xserve G5 cluster node comes with a 10 user license of Mac OS X Server installed.

Server Software Features

Here is a list of the key features of the system software on the Xserve G5. For information on installing or updating software, see the *Xserve G5 User's Guide*. For information on server topics, including server command line tools, refer to the Mac OS X Server Documentation website at http://www.apple.com/server/documentation.

■ **UPS support**: Mac OS X Server contains an enhanced version of UPS support that supports serial and USB UPS devices. The Power Manager has been enhanced to allow UPS vendors to communicate directly with the Power Manager to control their UPS hardware. UPS settings can be made in the Energy Saver preference pane and with the `pmset` command. See `man pmset` for more information.

The Server Monitor application shows status of the UPS.

An editable UPS shutdown script that will run when the machine powers down because of UPS is available in the `/user/libexec/upsshutdown` directory.

■ **Auto restart after power failure**: Xserve G5 hardware supports auto restart after power failure through software control. In the event of a power outage, an Xserve G5 unit detects the return of power and performs an automatic restart.

Also supported is staggered start-up after power failure, using the following terminal commands to alter the start-up times of a rack of machines by increments of 30 seconds to avoid overloading power.

`systemsetup -getwaitforstartupafterpowerfailure` — to get the number of seconds after which the computer will start up after a power failure.

`systemsetup -setwaitforstartupafterpowerfailure <seconds>` — to set the number of seconds after which the computer will start up after a power failure, where <seconds> must be a multiple of 30 seconds.

■ **Software administration tools**: The Administration Tools CD provides a rich set of tools for remote hardware monitoring and remote software management. The documentation ("man pages") for these tools is located in various subdirectories of the `/usr` directory. The Terminal application in Mac OS X provides access to a full array of command-line tools for software and system administration.

■ **Headless access**: If your Xserve G5 configuration does not include a video card and mouse, headless access is available through the command line. In a headless configuration, use the `softwareupdate` command to update your system software; refer to Command-Line Administration on the Mac OS X Server Documentation website.

■ **SNMP**: Implemented in Mac OS X Server, SNMP stack allows Xserve G5 monitoring by standard SNMP management consoles. In addition to the standard SNMP MIBs, Mac OS X Server provides MIBs for its core services. Xserve G5 also provides hardware MIBs for key values. SNMP support is currently read-only.

■ **Automatic NetBoot**: Xserve G5 can automatically invoke NetBoot by opening the drive handles. For information, refer to http://apple.com/server/documentation.

Security Features

Here are the key security features supported by the system software on the Xserve G5.

■ **Secure ports**: Xserve G5 prevents mounting of CDs as well as hot-plugged USB and FireWire hard drives by means of an enclosure lock.

■ **Secure remote management**: Xserve G5's remote monitoring and management tools run over encrypted links.

Storage Support

Here is a list of the key software features relating to hard disk storage on the Xserve G5.

■ **Disk utilities tool**: You can use the filesystem consistency check and interactive repair tool, included with Mac OS X, to work on the Xserve G5's file system. For more information, launch the Terminal application in Mac OS X and enter the following line after the prompt:

```
man diskutil
```

- **Remote volume configuration**: The system software can remotely configure newly mounted volumes.

- **USB and FireWire alerts**: Xserve G5's keyswitch security prevents unauthorized hot-plugging and mounting of a USB or FireWire hard drive. When the keyswitch is locked, the CD is ejected. In addition, the Security System pane provides configuration support for USB keyboard and mouse.

Management Support

Here are some of the management support features of the system software on the Xserve G5.

Command Line Tools

The following command line tools provide management support. Use the `man` command to display usage syntax.

systemsetup —to change the system preferences

networksetup — to change the network settings

pmset —to change the power management settings

SNMP Implementation

The SNMP implementation in Mac OS X Server allows the Xserve G5 to be monitored by standard SNMP management consoles.

The SNMP implementation on the Xserve G5 is based on the `net-snmp` project. For more information, see the `net-snmp` page on the World Wide Web at

http://www.net-snmp.com/

Computer Feature Identification

Rather than reading the box flag or the model string and then making assumptions about the server's features, applications that need to find out the features of the server should use IORegistry calls to test for the features they require. IORegistry calls are part of the I/O Kit API. For more information, see the references listed at "I/O Kit" (page 46).

Asset management software that reports the kind of computer it is running on can obtain the value of the model property from the device tree root node. The entry banner of the Open Firmware user interface software displays the model property. Or, to display the model property from within the Open Firmware user interface, type the following to display the model property:

```
0 > dev /
```

```
0 > .properties
```

The "dev /" selects the root device and ".properties" displays all properties of the device selected.

For both Xserve G5 configurations, the value of the model property is `RackMac3,1`.

Velocity Engine Acceleration

The Velocity Engine (an implementation of AltiVec) is the vector processing unit in the PowerPC G5 microprocessor. Some system software has been modified to take advantage of the accelerated processing that the Velocity Engine makes possible. System software has also been modified to support low-level operations using the Velocity Engine.

For complete information on the Velocity Engine, refer to the following Apple website:

http://developer.apple.com/hardwaredrivers/ve/index.html

Architecture

This chapter describes the architecture of the Xserve G5. It includes information about the major components on the logic boards: the microprocessor, the other main ICs, and the buses that connect them to each other and to the I/O interfaces.

Block Diagram and Buses

The architecture of Xserve G5 is based on one or two PowerPC G5 microprocessors and two custom ICs: the U3H memory controller and bus bridge and the K2 I/O controller. Figure 2-1 (page 22) is a simplified block diagram of a standard Xserve G5 with two PowerPC G5 microprocessors. The single microprocessor configuration and the cluster node configuration have similar structure with fewer features, as identified in Table 1-1 (page 11) and Table 1-2 (page 12) and throughout this developer note.

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Figure 2-1   Simplified block diagram
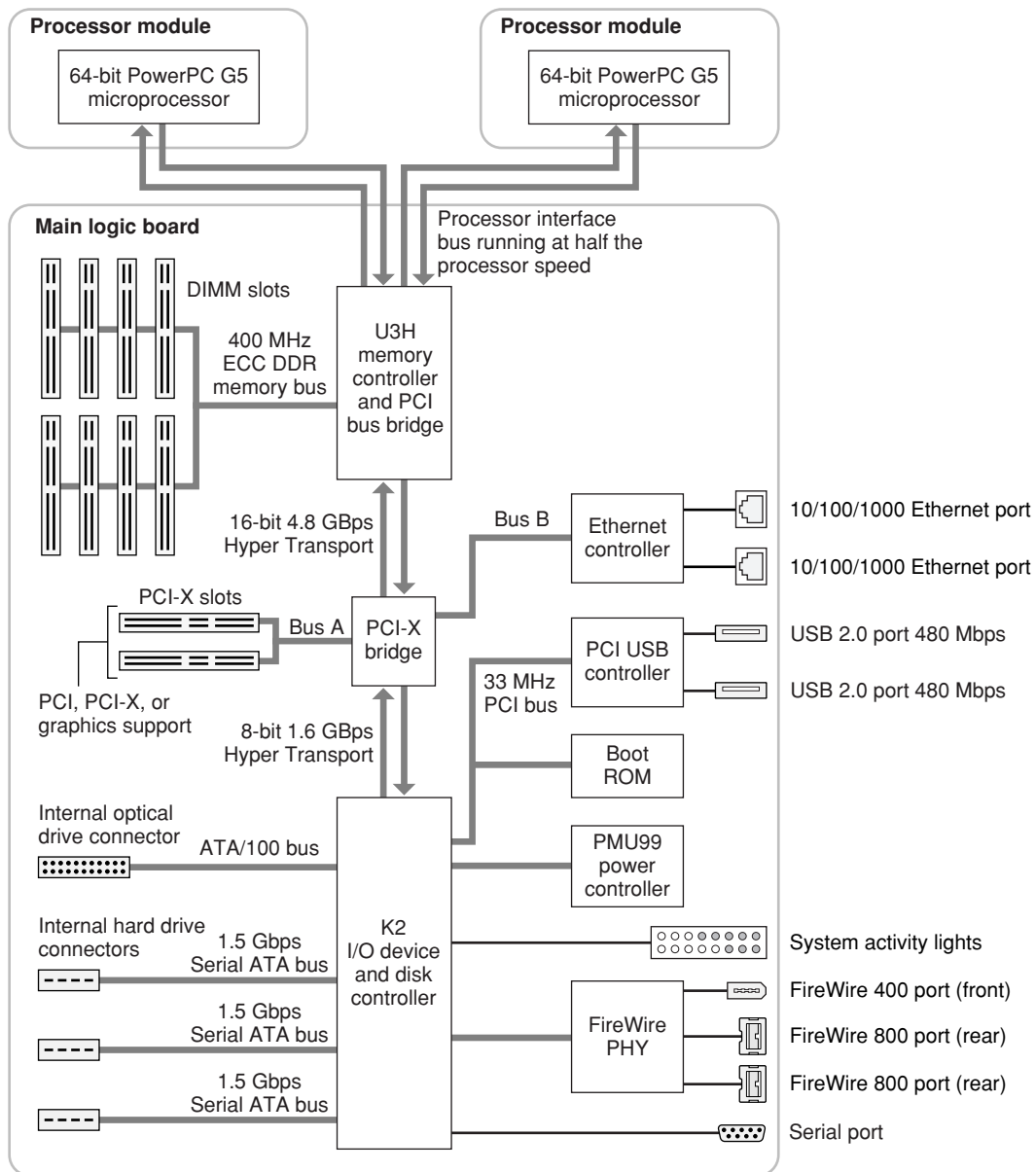
Xserve G5 has the following separate buses.

- Processor bus: running at half the speed of the processor, 64-bit data throughput per processor connecting the processor module to the U3H IC

- Dual processor systems have two independent, 64-bit processor buses, each running at half the speed of the processors

- Memory bus: 400 MHz, 128-bit bus connecting the main ECC DDR SDRAM memory to the U3H IC

- PCI-X bridge bus: supports two 64-bit PCI-X slots

- Internal PCI bus: 33 MHz, 32-bit bus supports the K2 I/O controller, the boot ROM, and the USB controllers

- Serial ATA (SATA) bus: supports 1.5 Gbps internal hard drive connectors

- Ultra DMA ATA/100 bus: support internal optical drive, where available

- HyperTransport: high-speed, bidirectional, point-to-point link for integrated circuits supports bidirectional data rates up to 4.8 GBps

The remainder of this chapter describes the architecture of the Xserve G5.

Processor Module

Depending on whether the Xserve G5 is a single or dual configuration, the processor module is one or two logic boards containing a G5 microprocessor. The processor module is connected to the main logic board by way of a 300-pin connector. To achieve the required level of performance, the signal lines that connect the processor module and the main logic board are carefully matched in length, loading, and impedance.

> ⚠️ **Warning:** DON'T TRY TO USE OLDER PROCESSOR CARDS! This connector differs from those in earlier computers and it is *not pin-compatible*.

PowerPC G5 Microprocessor

The PowerPC G5 used in the Xserve G5 has the following features:

- 64-bit PowerPC implementation with 42-bit physical memory addressing

- core runs at twice the bus speed

- superscalar execution core supporting more than 200 in-flight instructions

- two independent double-precision floating point units

- Velocity Engine: 128-bit-wide vector execution unit

- 64K L1 instruction cache, 32K L1 data cache per processor

- fully symmetric multiprocessing capability

- built-in 512KB L2 cache per processor

- independent, unidirectional frontside bus for each processor running at half the speed of the processor, each supporting a minimum of 8 GBps data throughput per processor

To find more information, see the reference at "PowerPC G5 Microprocessor" (page 45).

Cache Memory

The Xserve G5 has 512 KB L2 cache per processor built into the PowerPC G5 microprocessor.

> **Note:** The Xserve G5 does not use jumpers to control the clock speeds of the processor and cache.

Dual Processors

The dual-processor configurations of the Xserve G5 have two processor cards containing a PowerPC G5 processor. The dual-processor configurations allow applications that support multitasking to about double their performance.

> **Note:** The cluster node Xserve G5 is available only in dual configuration.

U3H Bridge and Memory Controller

The U3H custom IC is at the heart of the Xserve G5. It provides the bridging functionality among the processors, the memory system, and HyperTransport bus to the PCI-based I/O system.

Processor Bus

The processor bus runs at half the speed of the processor and connects the processor module to the U3H IC. The bus has 64-bit wide data and 36-bit wide addresses.

The Xserve G5 system controller is built with 130-nanometer, SOI technology, providing each subsystem with dedicated bandwidth to main memory. The Xserve G5 uses separate processor boards with each PowerPC G5 processor; two processor boards are used for dual processor systems. The U3H I/O implements two independent processor interfaces. The processor clock rate is up to 2.3 GHz in and connects to the U3H I/O through the Apple Processor Interface (API). The processor clock is derived from a PLL which multiplies the reference clock by preset intervals of 8 times.

Out-of-order completion allows the memory controller to optimize the data bus efficiency by transferring whichever data is ready, rather than having to pass data across the bus in the order the transactions were posted on the bus. This means that a fast DDR SDRAM read can pass a slow PCI read, potentially enabling the processor to do more before it has to wait on the PCI data.

Intervention is a cache-coherency optimization that improves performance for dual-processor systems. If one processor modifies some data, that data first gets stored only in that processor's cache. If the other processor then wants that data, it needs to get the new modified values.

Main Memory Bus

The Xserve G5 main memory bus connects the main memory to the U3H IC via the 64-bit data bus. Main memory is provided by up to eight ECC DDR400 (PC3200) SDRAM DIMMs. Supported DIMM sizes are 256 MB, 512 MB, and 1 GB. The DIMMs must be unbuffered and installed in pairs of the same size. The memory slots accept a maximum of eight 1 GB DIMMs for memory size of 8 GB.

For more information about memory DIMMs, see

HyperTransport Technology

The DDR HyperTransport is an advanced chip-to-chip communications technology that provides a high-speed, high-performance, point-to-point link for integrated circuits. HyperTransport provides a universal connection that reduces the number of buses within a system.

The HyperTransport bus between the U3H IC and the PCI-X bridge is 16 bits wide, supporting total of 4.8 GBps bidirectional throughput. Between the PCI-X bridge and the K2 IC, the bus width is 8 bits, supporting total of 1.6 GBps bidirectional throughput.

The HyperTransport bus supports two open PCI-X expansion slots for user expansion; see "PCI or PCI-X Expansion Slots" (page 25).

For more information on the HyperTransport technology, go to the World Wide Web at

http://www.hypertransport.org

PCI or PCI-X Expansion Slots

The Xserve G5 provides two open, user-accessible PCI-X slots via Bus A of the HyperTransport bus. Bus B implements the high speed, dual channel, on-board, gigabit Ethernet controller. To connect a monitor to the Xserve G5, Bus A also supports a build-to-order graphics card; see "Optional Graphics Card" (page 29).

Each user-accessible slot on Bus A has room for a full size 12.335-inch or short 6.926-inch card, holding a maximum of two full size cards.

The expansion slots on Bus A accommodate 32-bit and 64-bit PCI and PCI-X cards. PCI-X cards need to be compatible with Mac OS X and with PCI-X 1.0 standards. PCI cards need to be compatible with Mac OS X and with Xserve G5 systems. Supported PCI and PCI-X speeds are: 33 MHz, 66 MHz, 100 MHz, or 133 MHz. The 133 MHz PCI-X option is available only when one card is installed. If a second card is installed, the 133 MHz PCI-X card operates at a maximum of 100 MHz. If two cards are installed, both cards operate at the speed of the slower card. If a PCI card is installed in either slot, both slots will operate as PCI slots.

Important: The Xserve G5 must be powered off when installing or replacing PCI or PCI-X cards or a graphics card. Xserve G5 systems do not support PCI hot plug functionality.

The connectors to the PCI-X slots are 3.3 V keyed and support 32-bit and 64-bit buses. The connectors include a PME signal which allows a PCI card to wake the computer from sleep. Maximum power consumption for both expansion slots is 25 W (15 W top slot, 10 W bottom slot).

Note: 5 V keyed or signalling cards do not work in the Xserve G5.

The slots (12.335 inch) have a capture feature which is at the end of the slot. If a card exceeds the short length it is recommended that the long length be used rather than an intermediate length, to assure the card stays secure if and when the system is in shipment.

The U3H IC used in the Xserve G5 supports the PCI write combining feature. This feature allows sequential write transactions involving the Memory Write or Memory Write and Invalidate commands to be combined into a single PCI transaction. For memory write transactions to be combined, they must be sequential, ascending, and non-overlapping PCI addresses. Placing an `eieio` or `sync` command between the write commands prevents any write combining.

For more information, refer to "PCI and PCI-X Expansion Slots" (page 43).

Ethernet Controller

A separate Ethernet media access controller (MAC) and PHY support dual gigabit Ethernet. As a dedicated I/O channel on the dedicated PCI-X bus connected to the HyperTransport interface, it can operate at its full capacity without degrading the performance of other peripheral devices.

The MAC implements the link layer. It is integrated to a PHY interface that provides dual 10-BaseT, 100-BaseT, or 1000-BaseT operation over a standard twisted-pair interface. The operating speed of the link is automatically negotiated by the PHY and the bridge or router to which the Ethernet port is connected. For information about the port, see "Ethernet Ports" (page 35).

K2 I/O Controller

The K2 custom IC provides all the I/O functions. These functions are described in the following sections.

DMA Support

The K2 IC provides DB-DMA (descriptor-based direct memory access) support for the following I/O channels:

- Ultra ATA/100
- Communication slot interface
- I2S channel to the front panel display
- Serial ATA
- Firmware

The DB-DMA system provides a scatter-gather process based on memory-resident data structures that describe the data transfers. The DMA engine is enhanced to allow bursting of data files for improved performance.

Interrupt Support

The interrupt controller for the Xserve G5 system is an MPIC cell in the K2 IC. In addition to accepting K2 internal interrupt sources, the MPIC controller accepts internal interrupts from U3H and dedicated interrupt pins.

Internal PCI Bus

An internal 33-MHz, 64-bit PCI bus connects the K2 I/O controller to the boot ROM and the USB controller. The internal PCI bus offers no development opportunity.

Boot ROM

The boot ROM supports up to 2 MB of on-board flash EPROM. The boot ROM includes the hardware-specific code and tables needed to start up the computer. It uses Open Firmware to initialize the hardware, build the device tree, load an operating system, and provide common hardware access services.

PCI USB Controller

The Xserve G5 CPU uses a PCI USB controller ASIC with one Enhanced Host Controller Interface (EHCI) function and two Open Host Controller Interface (OHCI) functions. The controller has two external USB 2.0 ports. If connected to classic-speed USB devices, the two ports are connected to separate OHCI controllers.

The USB ports comply with the Universal Serial Bus Specification 2.0. The USB register set complies with the EHCI and OHCI specifications. For more information, see "USB Ports" (page 31).

Serial ATA Interface

Based on the Serial ATA 1.0 specification, Serial ATA (SATA) is a disk-interface technology that delivers up to 1.5 Gbps of performance to each independent drive on the Xserve G5. It provides a scalable, point-to-point connection that allows multiple ports to be aggregated into a single controller. Serial ATA uses a thin, point-to-point cable connection that enables easy routing within a system, avoiding master/slave, daisy-chaining, and termination issues and enabling better airflow within a system.

The K2 IC implements three Serial ATA revision one ports, each of which accommodates one independent internal hard drive.

For information about the drive bays, see "Hard Disk Drives" (page 38).

Serial Interface

The K2 IC implements an RS-232-compatible serial port for use with a terminal. See see "Serial Port" (page 36). You can use the RI input on the serial port connector to wake the Xserve G5 system from sleep mode.

Ultra DMA ATA/100 Interface

The K2 IC provides an Ultra DMA ATA/100 interface to support an optical drive. For information about optical drives, see "SuperDrive (Optional)" (page 38) or "Combo Drive" (page 37).

FireWire Controllers

The K2 IC includes a FireWire controller that supports both IEEE 1394b (FireWire 800) with a maximum data rate of 800 Mbps (100 MBps) and IEEE 1394a (FireWire 400) with a maximum data rate of 400 Mbps (50 MBps). The IC is backwards-compatible with 1394a (FireWire 400). The K2 IC provides DMA (direct memory access) support for the FireWire interface.

Two physical layer (PHY) ICs connected to the U3H IC implement the electrical signaling protocol for the FireWire ports. The FireWire 400 port is located on the front panel; two FireWire 800 ports are located on the back panel.

While the PHYs are operating, they act as repeaters so that the FireWire bus remains connected. For more information, see "FireWire Ports" (page 32).

> **Note:** The PHYs are powered even when the system is turned off, as long as the computer is connected to AC power.

Power Controller

The power management controller in Xserve G5 is a microcontroller called the PMU99. It supports several modes of power management that provide significantly lower power consumption than previous systems.

Dual System Monitor ICs

The Xserve G5 hardware contains an IC that monitors system voltages and the operation of both fans in the Xserve G5 enclosure. Voltages monitored include 5 V main, 12 V main, 3.3 V trickle, 2.5 V sleep, logic Vcore and processor Vcore. The system monitor IC also contains a built-in temperature sensor that measures the hardware's ambient temperature; a second sensor on the processor card measures local processor temperature. Software can access the system monitor IC through the second U3H IIC bus at port addresses 0x5A and 0x5C.

System Activity Lights

Two rows of eight lights indicate system activity. In a server with a single processor, the rows of system activity lights operate together; in a dual-processor server, the rows of lights operate independently to show each processor's activity. In that case, CPU 0 is shown by the top row, CPU 1 by the bottom.

Device Identification

Each Xserve G5 boot ROM contains a unique device serial number. However, because the boot ROM is a flash EPROM device, it is possible to overwrite the serial number and lose it irrecoverably. As an alternative, software that needs to identify an individual Xserve G5 can access the `local-mac-address` property of its Ethernet node, which is set by Open Firmware at boot time. You can read this property using a tool such as IORegistry Explorer.

Optional Graphics Card

The Xserve G5 has a build-to-order option of an ATI RV100 64 MB RAM VGA/PCI graphics card with a VGA connector. The ATI RV100 runs at 64-bit PCI 33 or 66 MHz.

The Xserve G5 can boot headless (that is, without an attached monitor). While booted headlessly, the system actually creates a virtual display and draws into an off-screen buffer, without attempting to update a physical display. It is important that application design take this condition into account and not assume that graphics activity implies that a user is present.

The Xserve G5 cluster node configuration does not have a graphics card or internal graphics and is accessed via remote command line.

For more information about the ATI RV100 VGA/PCI graphics card, see "VGA Connector" (page 39).

Input and Output Devices

This chapter describes the Xserve G5's built-in I/O devices and the ports for connecting external I/O devices. Each of the following sections describes an I/O port or device.

USB Ports

The Xserve G5 has two external Universal Serial Bus (USB) 2.0 ports. The USB ports are off of the USB controller connected to the PCI bus, bridged by K2. All USB ports are fully compliant with the USB 2.0 specification, including support for high-speed (480 Mbps) devices using an Enhanced Host Controller Interface (EHCI). Ports are automatically routed to a companion Open Host Controller Interface (OHCI) controller when a classic-speed (full-speed or low-speed) USB device is attached to a root hub port.

For low-speed and full-speed devices, the USB register set complies with the OHCI specification. For high-speed devices, the USB register set complies with the EHCI specification.
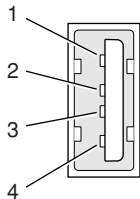
For more information about USB, refer to sources listed in "USB Interface" (page 48).

USB Connectors

The USB ports use USB Type A connectors, which have four pins each. Two of the pins are used for power and two for data. Figure 3-1 (page 31) shows the connector and Table 3-1 (page 32) shows the signals and pin assignments.

Figure 3-1   USB connector

Table 3-1   Signals on the USB connector

Pin	Signal name	Description
1	VCC	+5 VDC
2	D–	Data –
3	D+	Data +
4	GND	Ground

The Xserve G5 provides power for the USB ports at 5 V and up to 500 mA on each port. The ports share the same power supply; a short circuit on one will disable both ports until the short has been removed.

The USB ports support all USB 2.0 speeds: high-speed (480 Mbps) and classic USB speeds of full-speed (12 Mbps) and low-speed (1.5 Mbps). High-speed operation requires the use of shielded cables.

The Macintosh system software supports all four data transfer types defined in the USB specification.

FireWire Ports

The Xserve G5 has three external FireWire ports: two FireWire 800 on the rear panel of the enclosure and one FireWire 400 on the front. The bilingual FireWire 800 ports have 9-pin connectors and support transfer rates up to 800 Mbps; the FireWire 400 port has a 6-pin connectors and supports transfer rates of 100, 200, and 400 Mbps. As long as security is not engaged, the Xserve G5 can boot through FireWire; see "Booting from a FireWire Device" (page 35).

The FireWire ports

- provide a total of 15 watts of power when the computer system is on
- support up to 61 devices (each Xserve G5 has 2 internal devices)
- provide bus repeating capability as long as the computer is connected to AC power

The FireWire hardware and software provided with the Xserve G5 are capable of all asynchronous and isochronous transfers defined by IEEE standards 1394a and 1394b.

Developers of FireWire peripherals are required to provide device drivers. A driver for DV (digital video) is included in QuickTime 4.0 and later.

For more information about FireWire on Macintosh computers, please refer to the Apple FireWire website and the other sources listed in "FireWire Interface" (page 48).

FireWire 800 Connector

The FireWire 800 port on the Xserve G5 is based on IEEE 1394b and enables a 800 Mbps transfer rate. FireWire 800 uses a 9-pin connector and is backwards compatible with original 1394 FireWire devices with 6-pin or 4-pin connectors. With the appropriate cable, the 9-pin port works seamlessly with legacy FireWire devices. Cables are available to go from both 6-pin and 4-pin connectors to a 9-pin, and 9-pin to 9-pin.

Note: FireWire adapter cables are not included in the package.

The 9-pin FireWire 800 connector is shown in Figure 3-2 (page 33). Its connector signals and pin assignments are shown in Table 3-2 (page 33).

Figure 3-2   9-pin FireWire 800 connector
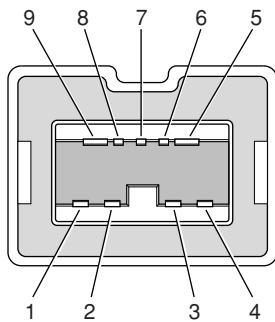
Table 3-2   Signals on the 9-pin FireWire 800 connector

Pin	Signal name	Description
1	TPB–	Twisted-pair B Minus
2	TPB+	Twisted-pair B Plus
3	TPA–	Twisted-pair A Minus
4	TPA+	Twisted-pair A Plus
5	TPA (R)	Twisted-pair A Ground Reference
6	VG	Power Ground
7	SC	Status Contact (no connection; reserved)
8	VP	Power Voltage (18 to 25 V DC)
9	TPB (R)	Twisted-pair B Ground Reference

VP (pin 8) provides up to 15 W power, shared with the other FireWire connectors. The voltage on the power pin is 18 to 25 V.

The 9-pin FireWire port is capable of operating at 100, 200, 400, and 800 Mbps, depending on the device it is connected to. Using a cable with a 9-pin connector at one end and a 4-pin or 6-pin connector at the other, the 9-pin port is capable of directly connecting to all existing FireWire devices. Using a cable with 9-pin connectors at both ends, the 9-pin port is capable of operating at 800 Mbps.

The IEEE 1394b standard defines long-haul media using Cat 5 UTP and several kinds of optical fiber. The Xserve G5 is interoperable with such cables but cannot be directly connected to them. To use long-haul cables, connect the computer to a 1394b hub that has the desired kind of long-haul connectors. If the hub has a bilingual port, that port can be connected to any of the computer's FireWire ports. If the hub has a beta-only port, it can be connected only to the computer's 9-pin port.

FireWire 400 Connector

The FireWire 400 port has a connector with six pins, as shown in Figure 3-3 (page 34). The connector signals and pin assignments are shown in Table 3-3 (page 34).

Figure 3-3   FireWire 400 connector
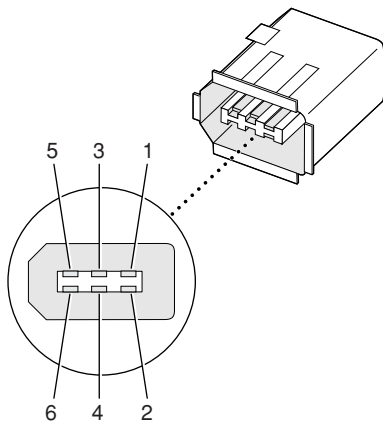
Table 3-3   Signals on the FireWire 400 connector

Pin	Signal name	Description
1	Power	Power (approximately 25 V DC)
2	Ground	Ground return for power and inner cable shield
3	TPB–	Twisted-pair B Minus
4	TPB+	Twisted-pair B Plus
5	TPA–	Twisted-pair A Minus
6	TPA+	Twisted-pair A Plus
Shell	—	Outer cable shield

The power pin provides up to 15 W total power for all three FireWire connectors. The voltage on the power pin can be from 18 to 25 V.

Pin 2 of the FireWire 400 connector is ground return for both power and the inner cable shield. In a FireWire cable with a 4-pin connector on the other end, the wire from pin 2 is connected to the shell of the 4-pin connector.

The signal pairs are crossed in the cable itself so that pins 5 and 6 at one end of the cable connect with pins 3 and 4 at the other end. When transmitting, pins 3 and 4 carry data and pins 5 and 6 carry clock; when receiving, the reverse is true.

Booting from a FireWire Device

Xserve G5 can boot from a FireWire storage device that implements SBP-2 (Serial Bus Protocol) with the RBC (reduced block commands) command set. Detailed information is available from Developer Technical Support: dts@apple.com.

For additional information about the FireWire interface and the Apple APIs for FireWire device control, see the references shown in

Ethernet Ports

The Xserve G5 provides dual, independent, gigabit Ethernet supporting 10Base-T, 100Base-T, and 1000Base-T transfer rates. In operation, the actual speed of each link is auto-negotiated between the computer's PHY device and the hub, switch, or router to which it the port is connected. Both the gigabit Ethernet card and the built-in gigabit Ethernet ports offer Jumbo Frame support.

Note: When connecting an Xserve G5 directly to another computer without using an Ethernet hub, a crossover cable is not required; circuits in the PHY detect the type of connection and switch the signal configuration as required.

The connectors for the Ethernet ports are RJ-45 connectors on the back of the computer. shows the signals and pin assignments for 10Base-T and 100Base-T operation. shows the signals and pin assignments for 1000Base-T operation.

Table 3-4   Signals for 10Base-T and 100Base-T operation

Pin	Signal name	Signal definition
1	TXP	Transmit (positive lead)
2	TXN	Transmit (negative lead)
3	RXP	Receive (positive lead)
4	–	Not used
5	–	Not used

Pin	Signal name	Signal definition
6	RXN	Receive (negative lead)
7	–	Not used
8	–	Not used

Table 3-5   Signals for 1000Base-T operation

Pin	Signal name	Signal definition
1	TRD+(0)	Transmit and receive data 0 (positive lead)
2	TRD–(0)	Transmit and receive data 0 (negative lead)
3	TRD+(1)	Transmit and receive data 1 (positive lead)
4	TRD+(2)	Transmit and receive data 2 (positive lead)
5	TRD–(2)	Transmit and receive data 2 (negative lead)
6	TRD–(1)	Transmit and receive data 1 (negative lead)
7	TRD+(3)	Transmit and receive data 3 (positive lead)
8	TRD–(3)	Transmit and receive data 3 (negative lead)

To interconnect two computers for 1000Base-T operation, you must use 4-pair cable (Category 5 or 6).

The Ethernet interface in the Xserve G5 conforms to the ISO/IEC 802.3 specification, where applicable, and complies with IEEE specifications 802.3i (10Base-T), 802.3u-1995 (100Base-T), and 802.3ab (1000Base-T).

Serial Port

The Xserve G5 has an RS-232-compatible serial port for connecting a terminal, using a standard DB-9 plug. Figure 3-4 (page 37) shows the mechanical arrangement of the pins on the serial port connector; Table 3-6 (page 37) shows the signal assignments.

The serial ports include a GPi (general-purpose input) signal on pin 7. The GPi signal connects to the data carrier detect input on the SCC (Serial Communications Controller). Alternatively, the GPi line can be connected to the receive/transmit clock (RTxCA) signal on the SCC. That connection supports devices that provide separate transmit and receive data clocks, such as synchronous modems.

Figure 3-4   Serial port connector
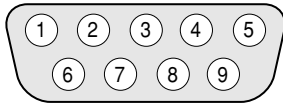
Table 3-6   Serial port signals

Pin	Signal name	Signal description
1	RLSD	Received line signal detector
2	RD	Received data
3	TD	Transmitted data
4	DRT	DTE ready
5	SGND	Signal ground
6	DCR	DCE ready
7	RTS	Request to send
8	CTS	Clear to send
9	RI	Ring indicator (wake up system)

Disk Drives

The standard Xserve G5 has three bay modules supporting up to three internal hard disk drives. The cluster node Xserve G5 has a single internal bay with one drive. Depending on the configuration purchased, some bays may be empty; empty bays are filled with blank drive carrier modules. The standard Xserve G5 also supports a Combo drive or a build-to-order SuperDrive.

Combo Drive

The standard Xserve G5 supports a slot-loading combination DVD-ROM and CD-RW drive.

The Combo drive can read DVD media and read and write CD media, as shown in Table 3-7 (page 37).

Table 3-7   Media read and written by the Combo drive

Media type	Reading speed	Writing speed
DVD-R	8x (CAV max)	–
DVD-ROM	8x (CAV max)	–

Media type	Reading speed	Writing speed
CD-R	24x (CAV max)	24x (ZCLV)
CD-RW	24x (ZCAV max)	16x (ZCLV, for Ultra speed media)
CD or CD-ROM	24x (CAV max)	–

SuperDrive (Optional)

The standard Xserve G5 supports an optional, slot-loading SuperDrive (combination DVD-R and CD-RW drive).

The SuperDrive can read DVD media and read and write CD media, as shown in Table 3-8.

Table 3-8   Media read and written by the SuperDrive

Media type	Reading speed (maximum)	Writing speed
DVD-R	6x (CAV max)	8x ZONE CLV, 4x/2x/1x (CLV) depending on media type
DVD-RW	6x (CAV max)	4x/2x/1x (CLV) depending on media type
DVD-ROM	8x (CAV max)	_
CD-R	24x (CAV max)	24x ZONE CLV
CD-RW	24x (CAV max)	14 (CLV) high speed CD-RW disc
CD or CD-ROM	24x (CAV max)	–

The Apple SuperDrive writes to DVD-R 4.7 gigabyte General Use media. These discs are playable in most standard DVD players and computer DVD-ROM drives.

For compatibility information regarding recordable DVD formats, refer to

http://dvddemystified.com/dvdfaq.html#4.3

Hard Disk Drives

The standard Xserve G5 enclosure has three drive bays for three fixed-media mass storage devices. For software applications, the bays are numbered one to three from left to right. In Open Firmware, the bays are numbered SD0 to SD2 from left to right. The cluster node Xserve G5 enclosure has a single drive bay on the left, which is referred to as 1 on the panel and SD0 in Open Firmware.

Note: Pin eleven supports the drive activity light. For full functionality of the drive activity light and system monitoring, use Apple drives. Other drives are not supported.

The drives on the independent Serial ATA buses implement revision one ports. For references to SATA website information, refer to "Serial ATA" (page 48).

Each drive carrier has two LEDs. The top one is a multicolor LED indicating drive state as follows:

■ Green: Drive in normal use by system

■ Yellow: Drive changing state (spinning up or down) or pre-failure warning

■ Red: Drive has failed

■ No color: No power to drive

The bottom (blue) LED indicates the individual drive's disk activity.

The monitoring software supports only drive modules manufactured by Apple.

VGA Connector

As a build-to-order option, the Xserve G5 slot load can have a video graphics card installed in Bus B of the PCI-X bridge. The card has a VGA connector for the video monitor.

The VGA connector is a three-row DB-15 (also called mini sub D15) connector for use with a VGA, SVGA, or XGA monitor. Figure 3-5 (page 39) shows the pin configuration and Table 3-9 (page 39) lists the signals and pin assignments.

Figure 3-5   VGA connector
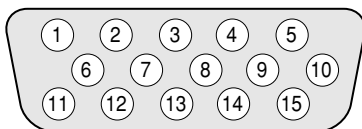
Table 3-9   Signals on the VGA connector

Pin	Signal name	Description
1	RED	Red video signal
2	GREEN	Green video signal
3	BLUE	Blue video signal
4	n.c.	No connect
5	GND	Ground
6	RED_RTN	Red video signal return

Pin	Signal name	Description
7	GREEN_RTN	Green video signal return
8	BLUE_RTN	Blue video signal return
9	n.c.	No connect
10	GND	Ground
11	n.c.	No connect
12	SDA	I2C data
13	HSYNC	Horizontal synchronization signal
14	VSYNC	Vertical synchronization signal
15	SCL	I2C clock

Expansion

This chapter describes the RAM expansion slots and the PCI expansion slots of the Xserve G5.

RAM Expansion

The main logic board of the Xserve G5 has four pairs of ECC DDR SDRAM expansion slots for unregistered, unbuffered DDR400 (PC3200) dual in-line memory modules (DIMMs) for a maximum memory of 8 GB.

The Xserve G5 has eight memory slots (in two banks for four each), at least two of which are filled at the factory. Additional DIMMs must be installed in pairs, starting with the slots closest to the center of the banks. Detailed instructions for installing additional memory modules are provided in the *Xserve G5 User's Guide* that shipped with your server.

To check the amount of DRAM installed, use Apple System Profiler (in Applications/Utilities).

DIMM Specifications

The RAM expansion slots accept 184-pin, unbuffered, ECC DDR400 SDRAM DIMMs that are 2.5 volt, unbuffered, 8-byte, with parity, and PC3200 compliant (3200 Mbytes/second bus bandwidth).

Mechanical Specifications

The mechanical design of the unbuffered ECC SDRAM DIMM is defined by the JEDEC specification JESD21-C, MODULES4_20_4, Release 11b. To find this specification on the World Wide Web, refer to

The maximum height of DIMMs for use in the Xserve G5 is 1.25 inches.

Electrical Specifications

The electrical design of the SDRAM DIMM is defined by the JEDEC specification JESD21-C, MODULES4_20_4, Release 11b. To find this specification on the World Wide Web, refer to

The Serial Presence Detect (SPD) EEPROM specified in the JEDEC standard is required and must be set to properly define the DIMM configuration. The EEPROM is powered on 2.5V. Details about the required values for each byte on the SPD EEPROM can be found on pages 68–70 of the JEDEC specification.

> **Important:** For a DIMM to be recognized by the startup software, the Serial Presence Detect feature must be programmed properly to indicate the timing modes supported by the DIMM.

DIMM Configurations

The largest DIMM supported is a two-bank DIMM of 1 GB using 512 Mbit unbuffered ECC DDR SDRAM devices. The maximum number of devices per DIMM is 18.

> **Important:** Power is delivered to the Xserve G5 system during sleep mode, so do not remove DIMMs while in sleep mode. A red light adjacent to the DIMMs is illuminated when power is still present.

Table 4-1 (page 42) shows information about the different sizes of unbuffered ECC DDR SDRAM devices used in the memory modules. The memory controller supports 64 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit ECC DDR SDRAM devices. The device configurations include three specifications: address range, word size, and number of banks. For example, a 1 M by 16 by 4 device addresses 1 M, stores 16 bits at a time, and has 4 banks.

The first column in Table 4-1 (page 42) shows the memory size of the largest DIMM with that device size that the computer can accommodate. The third column specifies the number of devices needed to make up the 8-byte width of the data bus. The fourth column in the table shows the size of each bank of devices, which is based on the number of internal banks in each device and the number of devices per bank.

Table 4-1   Sizes of ECC DDR SDRAM expansion DIMMS and devices

Size of DIMM	SDRAM device size	Device configuration	Devices per bank	Size of each bank
128 MB	128 Mbits	4 M x 8 x 4	9	64 MB
128 MB	256 Mbits	2 M x 16 x 4	5	64 MB
256 MB	128 Mbits	4 M x 8 x 4	9	128 MB
256 MB	256 Mbits	4 M x 16 x 4	5	128 MB
512 MB	256 Mbits	8 M x 8 x 4	9	256 MB
1 GB	512 Mbits	16 M x 8 x 4	9	512 MB

RAM Addressing

Signals A[0–12] on each SDRAM DIMM make up a 13-bit multiplexed address bus that can support several different sizes of SDRAM devices. Table 4-2 (page 43) shows the address multiplexing modes used with various devices.

Table 4-2   Address multiplexing modes for ECC DDR SDRAM devices

Device size	Device configuration	Size of row address	Size of column address
128 Mbits	4 M x 8 x 4	12	10
128 Mbits	2 M x 16 x 4	12	9
256 Mbits	8 M x 8 x 4	13	10
256 Mbits	4 M x 16 x 4	13	9
512 Mbits	8 M x 8 x 4	13	11

PCI and PCI-X Expansion Slots

The Xserve G5 provides Bus A and Bus B via the HyperTransport bus. Bus A provides the two slots for PCI or PCI-X expansion cards or an optional build-to-order graphics card. Bus B is dedicated gigabit Ethernet controller.

The Bus A expansion slots accept PCI or PCI-X cards at 33, 66, 100, or 133 MHz with either 32-bit or 64-bit address and data buses. The expansion slots support universal and +3.3 V cards, but not 5 V signalling. The cards are required to use the standard ISA fence described in the specification. The slots accept standard 6.88-inch and 12.283-inch

Note: 5 V keyed or signalling cards do not work in the Xserve G5.

The PCI-X configuration conforms to the PCI-X Specification 1.0. The PCI configuration is compatible with the PCI Specification 2.2.

To optimize performance of both PCI and main memory transfers, your PCI card should use DMA. The point-to-point G5 architecture is designed to provide optimal performance to each subsystem using DMA. If your card does not support DMA, it should use vector data types for read/write transfers. This approach results in 4 dword burst transfers on the PCI bus.

The computer's case has openings in the back for access to I/O connectors on the PCI-X cards. The cards are secured in place by thumb screws accessible from the back of the computer.

The expansion slots support all the required PCI signals and certain optional PCI signals. The PCI slots support the optional 64-bit data bus extension signals.

The maximum total power available for the two PCI-X slots is 30 watts.

Important: The user should first shut down the computer before removing or installing PCI-X expansion cards. Make sure the power light on the front is off. The Xserve G5 does not support PCI hot-plugging functionality.

For more information on PCI or PCI-X, visit the worldwide web at

http://www.pci-sig.org

PCI and PCI-X Expansion Slots

Supplemental Reference Documents

For more information about the technologies mentioned in this developer note, you may wish to consult some of the references listed in the following sections.

Apple Technical Notes

Apple Technical Notes answer many specific questions about the operation of Macintosh computers and the Mac OS. The technical notes are available on the Technical Note website at

http://developer.apple.com/technotes/

PowerPC G5 Microprocessor

Information about the PowerPC G5 microprocessor is available on the World Wide Web at

http://www-3.ibm.com/chips/techlib/techlib.nsf/productfamilies/PowerPC

Velocity Engine (AltiVec)

Velocity Engine is Apple's name for the AltiVec vector processor in the PowerPC G5 microprocessor. Apple provides support for developers who are starting to use the Velocity Engine in their applications. Documentation, development tools, and sample code are now available on the World Wide Web, at

http://developer.apple.com/hardwaredrivers/ve/index.html

Motorola's implementation of Apple's Velocity Engine is named AltiVec. The *AltiVec Technology Programming Environments Manual* (AltiVec PEM) is a reference guide for programmers. It contains a description for each instruction and information to help in understanding how the instruction works. You can obtain a copy of the AltiVec PEM through the Motorola documentation site on the World Wide Web, at

http://www.freescale.com/webapp/sps/site/overview.jsp?nodeId=02VS0l81285Nf2

Mac OS X and Mac OS Server

For access to Apple's developer documentation for Mac OS X, see the website at

http://developer.apple.com/documentation/MacOSX/MacOSX.html

and

http://developer.apple.com/documentation/Carbon/Reference/Multiprocessing_Services/

For information on Apple's server documentation for Mac OS X, see the website at

http://developer.apple.com/server/

O'Reilly & Associates publishes a series of books about Mac OS X development. The books in this series have been technically reviewed by Apple engineers and are recommended by the Apple Developer Connection.

I/O Kit

The I/O Kit is part of Darwin, the operating system foundation for Mac OS X. The documentation for I/O Kit is available on Apple's Darwin website at

http://developer.apple.com/documentation/Darwin/Darwin.html

ROM-in-RAM Architecture

The system software in all current Macintosh computers uses a ROM-in-RAM approach, also called the New World architecture. For more information about this architecture, see Technical Note 1167, *NewWorld Architecture*, available on Apple's technical note website at

http://developer.apple.com/technotes/tn/tn1167.html

Open Firmware

The software architecture implemented on current Macintosh computers follows the standard defined by the Open Firmware IEEE 1274-1994 specification. Three Technical Notes provide an introduction to Open Firmware on the Macintosh platform. They are

TN 1061: *Open Firmware, Part I*, available on the technical note web site at

http://developer.apple.com/technotes/tn/tn1061.html

TN 1062: *Open Firmware, Part II*, at

http://developer.apple.com/technotes/tn/tn1062.html

TN 1044: *Open Firmware, Part III*, at

http://developer.apple.com/technotes/tn/tn1044.html

Other technical notes provide additional information about Open Firmware on the Macintosh.

TN 2000: *PCI Expansion ROMs and You*, at

http://developer.apple.com/technotes/tn/tn2000.html

TN 2001: *Running Files from a Hard Drive in Open Firmware*, at

http://developer.apple.com/technotes/tn/tn2001.html

TN 2004: *Debugging Open Firmware Using Telnet*, at

http://developer.apple.com/technotes/tn/tn2004.html

RAM Expansion Modules

The Xserve G5 uses (DDR400) PC3200-compliant, 184-pin DDR SDRAM DIMMs.

The electrical and mechanical characteristics of the DIMM are given in JEDEC Standard 21-C. The specification can be found by using the search string JESD21-C on the Electronics Industry Association's website at

http://www.jedec.org/DOWNLOAD/default.cfm

ATA Devices

Information about ATA is available on the world wide web at

http://developer.apple.com/documentation/Hardware/DeviceManagers/ata/ata.html

Information about the ATA standards is available at the Technical Committee T13 AT Attachment website, at

http://www.t13.org/

Ethernet

For information on Ethernet specifications and design guides, go to the World Wide Web at

http://standards.ieee.org/

Serial ATA

For information on Serial ATA specifications and design guides, go to the World Wide Web at

http://www.serialata.org

USB Interface

For more information about USB on the Macintosh computer, refer to Apple Computer's *Accessing Hardware from Applications* at

http://developer.apple.com/documentation/HardwareDrivers/index.html

For full specifications of the Universal Serial Bus, you should refer to the USB Implementation Forum on the World Wide Web, at:

http://www.usb.org/developers/docs

FireWire Interface

For additional information about the FireWire 400 IEEE 1394a and FireWire 800 IEEE 1394b interfaces and the Apple APIs for FireWire software, refer to the resources available at

http://developer.apple.com/hardwaredrivers/firewire/index.html

The IEEE 1394a nd 1394b standards are available from the IEEE; you can order that document electronically from the IEEE Standards Department website at

http://shop.ieee.org/store

You may also find useful information at the 1394 trade association's website at

http://www.1394ta.org/

EIA Rack Standards

To obtain a copy of the Electronics Industries Association standard for 19-inch racks and cabinets, visit the site "Availability of EIA Standards and Technical Publications" at the following URL.

http://www.eia.org/technology/availability.phtml

Serial Interface Standards

The Telecommunications Industry Association (TIA) is the trade organization that publishes the standards for the RS-232 serial interface. To obtain copies of the standards, you can contact the TIA's web page at

http://www.tiaonline.org/standards/

Conventions and Abbreviations

This developer note uses the following typographical conventions and abbreviations.

Typographical Conventions

> **Note:** A note like this contains information that is of interest but is not essential for an understanding of the text.

> **Important:** A note like this contains important information that you should read before proceeding.

Abbreviations

When unusual abbreviations appear in this developer note, the corresponding terms are also spelled out. Standard units of measure and other widely used abbreviations are not spelled out.

Here are the standard units of measure used in developer notes:

A	amperes	mA	milliamperes
dB	decibels	A	microamperes
GB	gigabytes	MB	megabytes
Hz	hertz	MHz	megahertz
in.	inches	mm	millimeters
k	1000	ms	milliseconds
K	1024	s	microseconds
KB	kilobytes	ns	nanoseconds

kg	kilograms	sec.	seconds
kHz	kilohertz	V	volts
k	kilohms	W	watts
lb.	pounds		

Other abbreviations used in developer notes include these:

ADM	Apple drive module
ATA	advanced technology attachment
ATAPI	advanced technology attachment, packet interface
CAS	column address strobe
CD-ROM	compact disc read-only memory
CLI	command line interface
DBDMA	descriptor-based direct memory access
DDR	double data rate, a type of SDRAM
DIMM	dual inline memory module
DMA	direct memory access
DRAM	dynamic random-access memory
ECC	error code correction
EDO	extended data out DRAM device type
EIDE	extended IDE
EMI	electromagnetic interference
FTP	file transfer protocol
G5	Generation 5, the fifth generation of PowerPC microprocessors
GUI	graphic user interface
HID	human interface device, a class of USB devices
I2C	same as IIC
IIS	same as IIS
IC	integrated circuit
IDE	integrated device electronics

IEEE	Institute of Electrical and Electronics Engineers
IEEE 1274	the official specification for Open Firmware
IEEE 1394a	the official specification for FireWire 400
IEEE 1394b	the official specification for FireWire 800
IIC	inter-IC (an internal control bus)
IIS	inter-IC sound bus
I/O	input/output
ISO	International Organization for Standardization
JEDEC	Joint Electronics Devices Engineering Council
L2	level 2 (refers to level of cache)
LAN	local area network
MAC	media access controller
Mac OS	Macintosh Operating System
MIB	management infomation base
MPI	message passing interface
PCI	Peripheral Component Interconnect
PCI-X	Extended Peripheral Component Interconnect
PDC	primary domain controller
PHY	physical layer
PIO	polled input/output
RADIUS	Remote Authentication Dial-In User Service
RAID	redundant array of inexpensive drives
RAM	random-access memory
RAS	row address strobe
RBC	reduced block commands
RGB	a video signal format with separate red, green, and blue components
RISC	reduced instruction set computing
rms	root mean square

ROM	read-only memory
RS-232	standard serial interface
RS-422	standard serial interface
SBP	Serial Bus Protocol
SPD	Serial Presence Detect
SCSI	Small Computer System Interface
SCC	serial communications controller
SNMP	simple network management protocol
SDRAM	synchronous dynamic random access memory
SRAM	static random access memory
UPS	uninterruptible power supply
USB	Universal Serial Bus
VRAM	video RAM; used for display buffers

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